We claim:

1. In an integrated circuit chip including a plurality of metal layers and first and second supply potentials, a memory cell circuit for modification of a default register value, the circuit comprising:

a memory cell having

a first metal interconnect structure that traverses the plurality of metal layers using a first plurality of vias, wherein said first metal interconnect structure is coupled to one of said first and second supply potentials,

a second metal interconnect structure that traverses the plurality of metal layers using a second plurality of vias, wherein said second metal interconnect structure is coupled to the other one of said first and second supply potentials, and

an output, wherein a state of said output is programmable by altering any one of the plurality of metal layers or any one of a plurality of via layers;

a register having a data input, a data output and control inputs; and

a control circuit coupled to said control inputs of said register, wherein said control circuit receives a chip reset signal and said memory cell output to thereby force said data output of said register to a default register value that equals said output of said memory cell, regardless of said data input of said register.

2. The circuit of claim 1, wherein said control circuit comprises logic gates.

3. The circuit of claim 2, wherein said logic gates include a first and a second NAND gate and an inverter.

4. The circuit of claim 3, wherein said chip reset signal is input to said first and second NAND gates, said memory cell output is input to said second

NAND gate and said inverter, an output of said inverter is input to said first NAND gate, and outputs of said first and second NAND gates are provided to said control inputs of said register.

5. The circuit of claim 4, wherein said register comprises a flip-flop.

6. The circuit of claim 5, wherein said flip-flop comprises a D-Q flip-flop.

7. The circuit of claim 1, wherein prior to programming, said first and second metal interconnect structures are coupled at a top metal layer.

8. The circuit of claim 1, further comprising multiples of said first and second metal interconnect structures coupled together to form a plurality of programmable cycles for the memory cell, wherein each half cycle is programmable at least once.

9. The circuit of claim 8, wherein one cycle is laid out to form a ladder structure that traverses the plurality of metal layers from a bottom metal layer to a top metal layer and back to the bottom metal layer.

10. The circuit of claim 9, wherein said ladder structure is arranged to form a cube-shaped structure.

11. The circuit of claim 10, wherein the first and second supply potentials comprise two buses located in a central region of said cube-shaped structure and are accessible at each of the metal layers.

12. The circuit of claim 9, wherein said ladder structure is arranged to form a spiral-shaped structure.

13. The circuit of claim 12, wherein the first and second supply potentials comprise buses accessible at each of the metal layers.

14. The circuit of claim 1, wherein each of said first and second metal interconnect structures can be reprogrammed repeatedly by altering any one of the plurality of metal layers.

15. The circuit of claim 1, wherein each of said first and second metal interconnect structures can be reprogrammed repeatedly by altering any one of a plurality of via layers.

16. The circuit of claim 1, wherein each of said first and second metal interconnect structures can be reprogrammed repeatedly by altering any one of the plurality of metal layers and any one of a plurality of via layers.

17. The circuit of claim 1, wherein said first and second metal interconnect structures are not electrically coupled to each other at a top metal layer thereby forming two outputs for the memory cell.

18. The memory cell as in one of claims 14-17, wherein one of said first and second metal interconnect structures is coupled to the first supply potential at a bottom metal layer and the other of said first and second metal interconnect structures is coupled to the second supply potential at the bottom metal layer.

19. The circuit of claim 17, wherein said first and second metal interconnect structures are arranged to from a ladder structure.

20. The circuit of claim 17, wherein said first and second metal interconnect structures are arranged to from an offset ladder structure.

21. The circuit of claim 17, wherein said first and second metal interconnect structures are arranged to from a stacked structure.

22. The circuit of claim 21, wherein said stacked structure comprises first and second alternating metal interconnect patterns.

23. The circuit of claim 22, wherein:

said first alternating metal interconnect pattern comprises first and second interspersed metal traces, and

said second alternating metal interconnect pattern comprises third and fourth interspersed metal traces, and

wherein said third and fourth interspersed metal traces form a mirror image of first and second interspersed metal traces.

24. The circuit of claim 23, wherein said first plurality of vias interconnect ones of said first and third interspersed metal traces and said second plurality of vias interconnect ones of said second and fourth interspersed metal traces.

25. The circuit of claim 23, wherein the memory cell is programmed at any metal layer by forming an open circuit in each of said first and second interspersed metal traces of that layer thereby splitting each metal trace into two portions, and coupling together a first portion of said first interspersed metal trace to a first portion of said second interspersed metal trace and coupling together a second portion of said first interspersed metal trace to a second portion of said second interspersed metal trace.

26. The circuit of claim 25, wherein said open circuits and coupling is not performed in regions where vias are located.

27. The circuit of claim 26, wherein said programming is reversible during a subsequent chip revision.

28. The circuit of claim 24, wherein the memory cell is programmed at any of a plurality of via layers by removing two vias and inserting two vias.

29. The circuit of claim 28, wherein said programming is reversible during a subsequent chip revision.

30. The memory cell as in one of claims 26-28, wherein one of said first and second metal interconnect structures is coupled to the first supply potential at a bottom metal layer and the other of said first and second metal interconnect structures is coupled to the second supply potential at the bottom metal layer.